

LDEED3330KA5N00

Aliases (DEED3330KA5N00)

LDE, Film, Metallized PEN Stacked, Automotive Grade, 0.33 uF, 10%, 100 VDC, 63 VAC, 125°C, 2220, 3.3mm



Click [here](#) for the 3D model.

Dimensions

Chip Size	2220
L	6mm +/-0.3mm
W	5mm +/-0.4mm
T	3.3mm MAX
B	0.4mm +0.5/-0.3mm

Packaging Specifications

Packaging	T&R
Packaging Quantity	2250

General Information

Series	LDE
Dielectric	Metallized PEN Stacked
Style	SMD Chip
Features	Automotive Grade
RoHS	Yes
Qualifications	AEC-Q200
AEC-Q200	Yes
Typical Component Weight	0.356 g
Shelf Life	104 Weeks
MSL	3

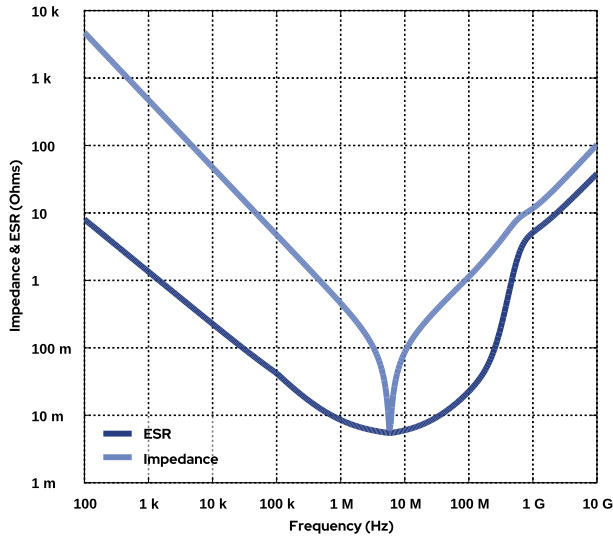
Specifications

Capacitance	0.33 uF
Capacitance Tolerance	10%
Voltage DC	100 VDC
Voltage AC	63 VAC
Temperature Range	-55/+125°C
Rated Temperature	125°C
Dissipation Factor	0.8% 1kHz
Insulation Resistance	1 GOhms
Max dV/dt	100 V/us

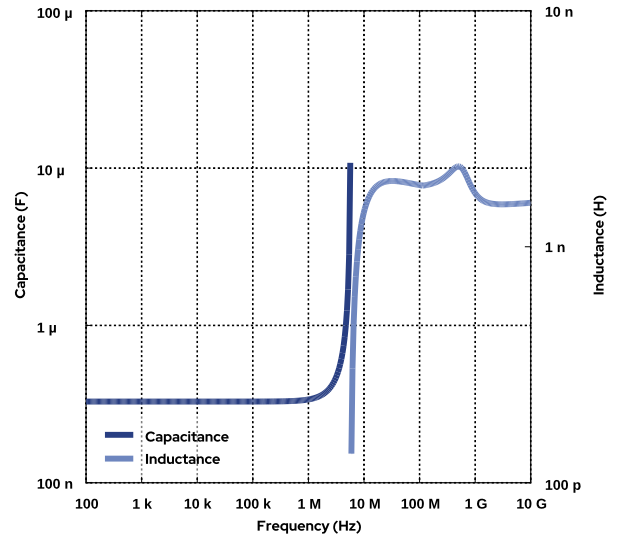
Simulations

For the complete simulation environment please visit [K-SIM](#).

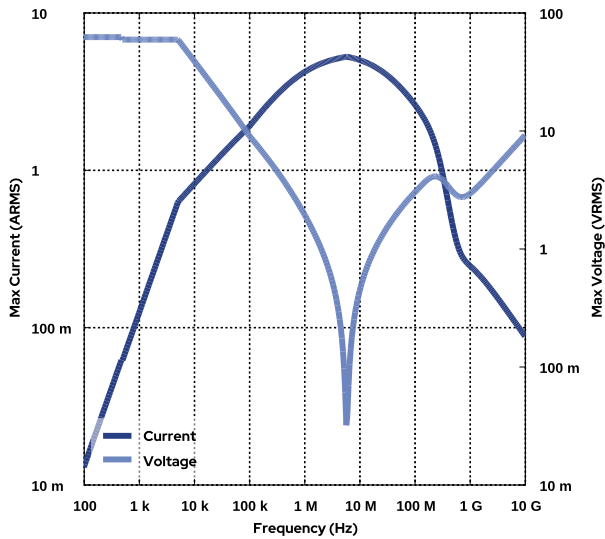
Impedance and ESR



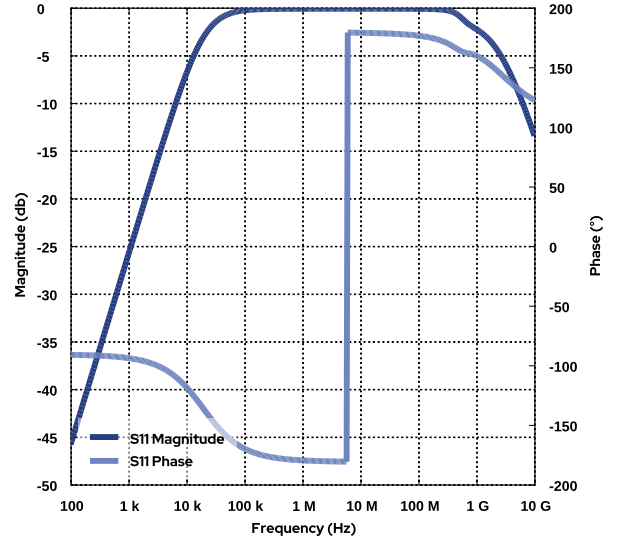
Capacitance and Inductance

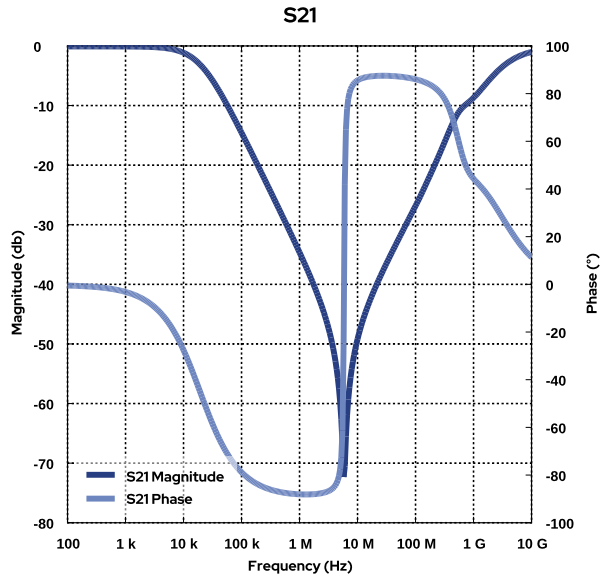


Current and Voltage



S11





These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.