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General Information

Series	KPS LDD Mil SMPS PRF49470
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current
RoHS	No
Prop 65	WARNING: Cancer and reproductive harm - https://www.p65warnings.ca.gov/
Termination	60/40 Solder Coated
Lead	J Leads
Failure Rate	N/A
Testing and Reliability	Level T
Qualifications	MIL-PRF-49470
AEC-Q200	No
Notes	Note: Number of chips in stack depends on design. Note: Turn Radius For Lead Extension Is 0.1 Radians (Typical). Note: Lead alignment within pin rows shall be within ± 0.13 mm.

Dimensions

D	25.715mm +/-1.585mm
L	1.78mm +/-0.25mm
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	6.096mm MAX
C	11.43mm +/-0.635mm
E	12.7mm MAX
LO	1.586mm MAX
LW	0.508mm +/-0.051mm
MP	1.27mm MIN

Packaging Specifications

Packaging	Waffle, Box
Packaging Quantity	28

Specifications

Capacitance	5.6 uF
Tolerance	10%
Voltage DC	200 VDC
Dielectric Withstanding Voltage	500 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	BR
Dissipation Factor	2.5%
Insulation Resistance	178.571 MOhms

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