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Dimensions	
D	13.5mm MAX
L	6.35mm MIN
H	2.54mm +/-0.127mm
F	1.397mm +/-0.25mm
A	6.6mm MAX
B	8.64mm MAX
C	6.35mm +/-0.635mm
E	7.62mm MAX
K	0.5mm +/-0.05mm

Packaging Specifications	
Packaging	Waffle, Box
Packaging Quantity	50

General Information	
Series	KPS-MCL Indust COG HT200C
Style	Leaded Stacked Chip
Description	Low Loss, Low ESR, Stacked Ceramic Chips
Features	200C, Low ESR, High Thermal Stability, Bulk Capacitance
RoHS	With Exemptions
REACH	SVHC (Pb – CAS 7439-92-1)
SCIP Number	297427bb-2a48-4853-b594-641304a2cc24
Termination	Silver
Lead	Straight Leads
AEC-Q200	No
Notes	Number of chips in this stack: 5.

Specifications	
Capacitance	0.09 uF
Capacitance Tolerance	10%
Voltage DC	1000 VDC
Dielectric Withstanding Voltage	1200 VDC
Temperature Range	-55/+200°C
Temperature Coefficient	COG
Dissipation Factor	0.1% 1 kHz 25C
Aging Rate	0% Loss/Decade Hour
Insulation Resistance	11.11 GOhms

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