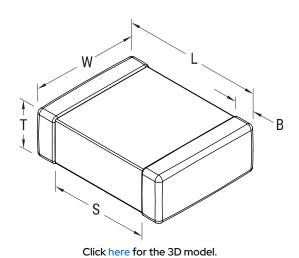


C0402C225K7PACTU

Aliases (C0402C225K7PAC7867) SMD Comm X5R, Ceramic, 2.2 uF, 10%, 4 VDC, X5R, SMD, MLCC, Temperature Stable, Class II, 0402, 0.3 mm



General Information Series SMD Comm X5R Style SMD Chip SMD, MLCC, Temperature Stable, Class II Description Features Temperature Stable, Class II RoHS Yes Termination Tin Marking No AEC-Q200 No **Typical Component Weight** 1.21 mg Shelf Life 78 Weeks MSL 1

	Specifications	
_	Capacitance	2.2 uF
	Measurement Condition	1 kHz 0.5Vrms
	Tolerance	10%
	Voltage DC	4 VDC
	Dielectric Withstanding Voltage	10 VDC
	Temperature Range	-55/+85°C
	Temp. Coefficient	X5R
1	Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	15%, 1kHz 0.2Vrms
	Dissipation Factor	10% 1 kHz 0.5Vrms
	Aging Rate	5% Loss/Decade Hour: Referee Time is 48 Hours
	Insulation Resistance	45.5 MOhms

 Dimensions

 Chip Size
 0402

 L
 1mm +/-0.05mm

 W
 0.5mm +/-0.05mm

 T
 0.5mm +/-0.05mm

 S
 0.3mm MIN

 B
 0.3mm +/-0.1mm

Packaging Specifications

Packaging T&R, 180m	m, Paper Tape
Packaging Quantity 10000	

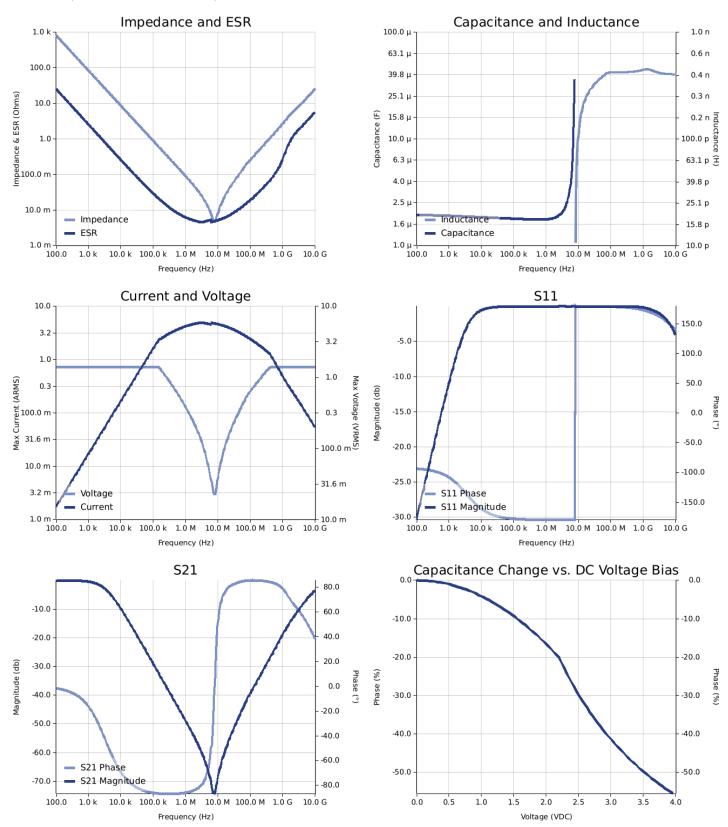
Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute – and we specifically disclaim – any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.



CO402C225K7PACTU Aliases (C0402C225K7PAC7867) SMD Comm X5R, Ceramic, 2.2 uF, 10%, 4 VDC, X5R, SMD, MLCC, Temperature Stable, Class II, 0402, 0.3 mm

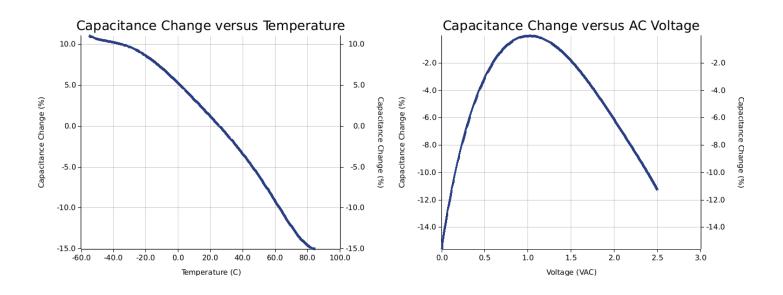
Simulations

For the complete simulation environment please visit K-SIM.





CO402C225K7PACTU Aliases (C0402C225K7PAC7867) SMD Comm X5R, Ceramic, 2.2 uF, 10%, 4 VDC, X5R, SMD, MLCC, Temperature Stable, Class II, 0402, 0.3 mm





These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.

- The ESR used for hipple klipple current younge vs. requericy plots is the ESR at an bient temperature.
 The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
 The effects shown herein are based on measured data from a multiple part sample of the parts in question.
 Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
 The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages are applied to reach previous the burger of the parts.
- generated at any other harmonics. Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.