

HV-HT Series, High Voltage, High Temperature 200°C, COG Dielectric, 500 – 2,000 VDC (Industrial Grade)

Overview

KEMET's High Voltage-High Temperature (HV-HT) series surface mount COG Multilayer Ceramic Capacitors (MLCCs) are constructed of a robust and proprietary base metal electrode (BME) dielectric system that offers industry-leading performance at extreme temperatures. These surface mountable devices feature a 200°C maximum operating temperature and are specifically designed to withstand the demands of harsh industrial environments such as oil exploration and automotive/avionics engine compartment circuitry. They also offer higher and more uniform breakdown voltage performance than competitive products, resulting in increased yields in customer field applications. When dealing with expensive high temperature circuitry and systems, higher yields can quickly result in significant cost savings.

KEMET's HV-HT series MLCCs are temperature compensating and are suited for resonant circuit applications or those where Q and stability of capacitance characteristics are required. They exhibit no change in

capacitance with respect to time and voltage and boast a negligible change in capacitance with reference to ambient temperature. Capacitance change is limited to $\pm 30\text{ppm}/^\circ\text{C}$ from -55°C to $+200^\circ\text{C}$. In addition, these capacitors exhibit high insulation resistance with low dissipation factor at elevated temperatures up to 200°C. They also exhibit low ESR at high frequencies and offer superior volumetric efficiency over competitive high temperature precious metal electrode (PME) and base metal electrode (BME) dielectric system devices.

These devices are Lead (Pb)-free, RoHS and REACH compliant without the need of any exemptions.



Ordering Information

C	2225	H	393	J	C	G	A	C	TU
Ceramic	Case Size (L" x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance ¹	Rated Voltage (VDC)	Dielectric	Failure Rate/ Design	Termination Finish ²	Packaging/ Grade (C-Spec)
	0805 1206 1210 1808 1812 1825 2220 2225 2824 3040 3640 4540	H = High temperature (200°C)	Two significant digits and number of zeros.	B = ± 0.10 pF C = ± 0.25 pF D = ± 0.5 pF F = $\pm 1\%$ G = $\pm 2\%$ J = $\pm 5\%$ K = $\pm 10\%$ M = $\pm 20\%$	C = 500 B = 630 D = 1,000 F = 1,500 G = 2,000	G = COG	A = N/A	C = 100% Matte Sn L = SnPb (5% Pb minimum) E = Gold (Au) 1.97 – 11.8 μin F = Gold (Au) 30 – 70 μin G = Gold (Au) 100 μin minimum	See "Packaging C-Spec Ordering Options Table"

¹ Additional capacitance tolerance offerings may be available. Contact KEMET for details.

² Gold(Au) termination finish options are not available on 2824, 3040, 3640 and 4540 case sizes.

Packaging C-Spec Ordering Options Table

Termination Finish Options	Packaging Type/Options	Packaging Ordering Code (C-Spec)
Standard Packaging – Unmarked³		
C = 100% Matte Sn L = SnPb (5% Pb min.) F = Gold (Au) 30 – 70 µin G = Gold (Au) 100 µin minimum	Bulk Bag	Blank ¹
	Waffle Tray ²	7292
	7" Tape & Reel	TU
	13" Reel	7411 (EIA 0603 and smaller case sizes) 7210 (EIA 0805 and larger case sizes)
	7" Tape & Reel – 50 pcs	T050
	7" Tape & Reel – 100 pcs	T100
	7" Tape & Reel – 250 pcs	T250
	7" Tape & Reel – 500 pcs	T500
7" Tape & Reel – 1,000 pcs	T1K0	
Moisture Sensitive Packaging⁴ – Unmarked³		
E = Gold (Au) 1.97 – 11.8 µin F = Gold (Au) 30 – 70 µin G = Gold (Au) 100 µin minimum	Waffle Tray ²	7282
	7" Tape & Reel	7130
	7" Tape & Reel – 50 pcs	Contact KEMET ⁵
	7" Tape & Reel – 100 pcs	
	7" Tape & Reel – 250 pcs	
	7" Tape & Reel – 500 pcs	
7" Tape & Reel – 1,000 pcs		

¹ Default packaging is "Bulk Bag". An ordering code C-Spec is not required for "Bulk Bag" packaging.

¹ "Bulk Bag" packaging option is not available for Gold (Au) termination finish options and case sizes larger than 2225 (5664 Metric).

² "Waffle Tray" packaging option is not available for case sizes larger than 2225 (5664 Metric).

³ The terms "Marked" and "Unmarked" pertain to laser marking option of components. All packaging options labeled as "Unmarked" will contain capacitors that have not been laser marked. The option to laser mark is not available on these devices.

³ Reeling quantities are dependent upon chip size and thickness dimension. When ordering using the "T1K0" packaging option, 1812 through 2225 case size devices with chip thickness of $\geq 1.9\text{mm}$ (nominal) may be shipped on multiple 7" reels or a single 13" reel. Additional reeling or packaging options may be available. Contact KEMET for details.

⁴ Moisture sensitive packaging is required for Gold (Au) termination option "E" (1.97 µin min / 11.8 µin max.). Not available for case sizes larger than 2225 (5664 Metric).

⁵ Additional reeling or packaging options may be available. Contact KEMET for details.

Benefits

- Operating temperature range of -55°C to +200°C
- Lead (Pb)-free, RoHS, and REACH compliant
- EIA 0805, 1206, 1210, 1808, 1812, 1825, 2220, 2225, 2824, 3040, 3640, and 4540 case sizes
- DC voltage ratings of 500 V, 630 V, 1 KV, 1.5 KV, and 2 KV
- Capacitance offerings ranging from 1 pF to 0.150 µF
- Available capacitance tolerances of ±0.10 pF, ±0.25 pF, ±0.5 pF, ±1%, ±2%, ±5%, ±10%, and ±20%
- No piezoelectric noise
- Extremely low ESR and ESL
- High thermal stability
- High ripple current capability
- No capacitance change with respect to applied rated DC voltage
- Negligible capacitance change with respect to temperature from -55°C to +125°C
- No capacitance decay with time
- Non-polar device, minimizing installation concerns
- 100% pure matte tin-plated termination finish allowing for excellent solderability
- SnPb plated termination finish option available upon request (5% Pb minimum)
- Gold (Au), Tin/Lead (Sn/Pb) and 100% pure matte Tin (Sn) termination finishes available

Applications

Typical applications include critical timing, tuning, circuits requiring low loss, circuits with pulse, high current, switch mode power supplies (input filters, resonators, tank circuits, snubbed circuits, output filters), high voltage coupling, DC blocking and voltage multiplier circuits in extreme environments such as down-hole exploration, aerospace engine compartments and geophysical probes. Markets include power supply, HID lighting, industrial equipment/control, automotive, aerospace, and munitions.

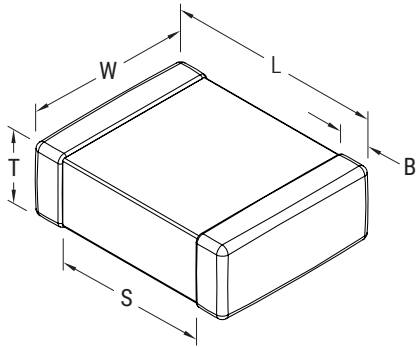
Qualification/Certification

High temperature (200°C) Industrial grade products meet or exceed the requirements outlined in Table 4, Performance & Reliability. Qualification packages are available for review and download on our website at www.kemet.com/hightemp

Environmental Compliance

Lead (Pb)-free, RoHS, and REACH compliant without exemptions (excluding SnPb termination finish option).

Dimensions – Millimeters (Inches)



EIA Size Code	Metric Size Code	L Length	W Width	T Thickness	B Bandwidth	S Separation Minimum	Mounting Technique
0805	2012	2.00 (0.079) ±0.20 (0.008)	1.25 (0.049) ±0.20 (0.008)	See Table 2 for Thickness	0.50 (0.02) ±0.25 (0.010)	0.70 (0.028)	Solder Wave or Solder Reflow
1206	3216	3.20 (0.126) ±0.20 (0.008)	1.60 (0.063) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)	1.50 (0.060)	
1210	3225	3.20 (0.126) ±0.20 (0.008)	2.50 (0.098) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)	1.50 (0.060)	Solder Reflow Only
1808	4520	4.70 (0.185) ±0.50 (0.020)	2.00 (0.079) ±0.20 (0.008)		0.60 (0.024) ±0.35 (0.014)	2.90 (0.114)	
1812	4532	4.50 (0.177) ±0.30 (0.012)	3.20 (0.126) ±0.30 (0.012)		0.60 (0.024) ±0.35 (0.014)	2.30 (0.091)	
1825	4564	4.50 (0.177) ±0.30 (0.012)	6.40 (0.252) ±0.40 (0.016)		0.60 (0.024) ±0.35 (0.014)	2.30 (0.091)	
2220	5650	5.70 (0.224) ±0.40 (0.016)	5.00 (0.197) ±0.40 (0.016)		0.60 (0.024) ±0.35 (0.014)	3.50 (0.138)	
2225	5664	5.60 (0.220) ±0.40 (0.016)	6.40 (0.248) ±0.40 (0.016)		0.60 (0.024) ±0.35 (0.014)	3.20 (0.126)	
2824	7260	7.10 (0.280) ±0.40 (0.016)	6.10 (0.240) ±0.40 (0.016)		1.27 (0.050) ±0.40 (0.016)	4.20 (0.165)	
3040	7610	7.60 (0.300) ±0.40 (0.016)	10.20 (0.402) ±0.40 (0.016)		1.27 (0.050) ±0.40 (0.016)	4.20 (0.165)	
3640	9210	9.10 (0.358) ±0.40 (0.016)	10.20 (0.402) ±0.40 (0.016)		1.27 (0.050) ±0.40 (0.016)	6.30 (0.248)	
4540	-	11.40 (0.449) ±0.40 (0.016)	10.20 (0.402) ±0.40 (0.016)		1.27 (0.050) ±0.40 (0.016)	6.30 (0.248)	

Table 1A – Capacitance Range/Selection Waterfall (0805 – 1808 Case Sizes) cont.

Capacitance	Cap Code	Case Size/Series	C0805H			C1206H					C1210H					C1808H					
		Voltage Code	C	B	D	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G	
		Rated Voltage (VDC)	500	630	1000	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000	
		Capacitance Tolerance	Product Availability and Chip Thickness Codes See Table 2 for Chip Thickness Dimensions																		
5,100 pF	512														FY	FS					LA
5,600 pF	562														FY	FS					LB
6,200pF	622														FY						LC
6,800pF	682														FY						LC
7,500pF	752														FS						
8,200 pF	822														FS						
Capacitance	Cap Code	Rated Voltage (VDC)	500	630	1000	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000	
		Voltage Code	C	B	D	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G	
		Case Size/Series	C0805H			C1206H					C1210H					C1808H					

*Capacitance range Includes E24 decade values only. (i.e., 10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, and 91)
 KEMET reserves the right to substitute product with an improved temperature characteristic, tighter capacitance tolerance and/or higher voltage capability within the same form factor (configuration and dimensions).
 These products are protected under US Patents 7,172,985 and 7,670,981, other patents pending, and any foreign counterparts.

Table 1B – Capacitance Range/Selection Waterfall (1812 – 2225 Case Sizes) cont.

Capacitance	Cap Code	Case Size/Series	C1812H					C1825H					C2220H					C2225H													
		Voltage Code	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G									
		Rated Voltage (VDC)	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000									
Capacitance Tolerance		Product Availability and Chip Thickness Codes See Table 2 for Chip Thickness Dimensions																													
5,100 pF	512	F	G	J	K	M	GH	GK	GO				HG	HE	HG	HK				JK	JK	JK	JL			KE	KF	KF	KH		
5,600 pF	562	F	G	J	K	M	GH	GK	GO				HG	HE	HG	HK				JK	JK	JK	JN			KE	KF	KF	KH		
6,200pF	622	F	G	J	K	M	GH	GK					HG	HE	HG				JK	JE	JE	JN			KE	KF	KF	KJ			
6,800pF	682	F	G	J	K	M	GH	GM					HG	HE	HJ				JK	JE	JK	JN			KE	KF	KF	KJ			
7,500pF	752	F	G	J	K	M	GH	GM					HG	HE	HJ				JK	JE	JK				KF	KE	KF				
8,200 pF	822	F	G	J	K	M	GK	GO					HG	HE	HJ				JK	JE	JL				KF	KE	KF				
9,100 pF	912						GM	GO					HE	HG	HK				JE	JE	JL				KF	KE	KH				
10,000 pF	103						GM	GO					HE	HG	HK				JE	JE	JL				KF	KE	KH				
12,000 pF	123						GO						HE	HG					JE	JK	JN				KE	KE	KH				
15,000 pF	153						GO						HE	HJ					JE	JL					KE	KF	KJ				
18,000 pF	183												HG	HK					JE	JL					KE	KH					
22,000 pF	223												HJ						JK	JN					KF	KJ					
27,000 pF	273												HJ						JL	JN					KF	KJ					
33,000 pF	333												HK						JN						KH	KJ					
39,000 pF	393																								KJ						
Capacitance	Cap Code	Rated Voltage (VDC)	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000									
		Voltage Code	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G									
		Case Size/Series	C1812H					C1825H					C2220H					C2225H													

*Capacitance range Includes E24 decade values only. (i.e., 10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, and 91)
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Table 1C – Capacitance Range/Selection Waterfall (2824 – 4540 Case Sizes)

Capacitance	Cap Code	Case Size/ Series			C2824H					C3040H					C3640H					C4540H				
		Voltage Code			C	B	D	F	G	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G
		Rated Voltage (VDC)			500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000
		Capacitance Tolerance			Product Availability and Chip Thickness Codes See Table 2 for Chip Thickness Dimensions																			
10 - 2,000 pF	100 - 202	J	K	M																				
2,200 pF	222	J	K	M	TA	TA	TA	TA	TA															
2,400 pF	242	J	K	M																				
2,700 pF	272	J	K	M	TA	TA	TA	TA	TA															
3,000 pF	302	J	K	M																				
3,300 pF	332	J	K	M	TA	TA	TA	TA	TA	QB	QB	QB	QB	QB										
3,600 pF	362	J	K	M																				
3,900 pF	392	J	K	M	TA	TA	TA	TA	TB	QB	QB	QB	QB	QB	MA	MA	MA	MA	MA					
4,300 pF	432	J	K	M																				
4,700 pF	472	J	K	M	TA	TA	TA	TB	TB	QB	QB	QB	QB	QB	MA	MA	MA	MA	MA	SA	SA	SA	SA	SA
5,100 pF	512	J	K	M																				
5,600 pF	562	J	K	M	TA	TA	TA	TB	TC	QB	QB	QB	QB	QB	MA	MA	MA	MA	MA	SA	SA	SA	SA	SA
6,200 pF	622	J	K	M																				
6,800 pF	682	J	K	M	TA	TA	TA	TB		QB	QB	QB	QB	QC	MA	MA	MA	MA	MA	SA	SA	SA	SA	SA
7,500 pF	752	J	K	M																				
8,200 pF	822	J	K	M	TA	TA	TA	TC		QB	QB	QB	QC	QC	MA	MA	MA	MA	MB	SA	SA	SA	SA	SA
9,100 pF	912	J	K	M																				
10,000 pF	103	J	K	M	TA	TA	TA			QB	QB	QB	QC	QD	MA	MA	MA	MA	MB	SA	SA	SA	SA	SB
12,000 pF	123	J	K	M	TA	TA	TA			QB	QB	QB	QD		MA	MA	MA	MB	MB	SA	SA	SA	SA	SB
15,000 pF	153	J	K	M	TA	TA	TB			QB	QB	QB	QD		MA	MA	MA	MB	MC	SA	SA	SA	SB	SB
18,000 pF	183	J	K	M	TA	TA	TB			QB	QB	QB			MA	MA	MA	MC		SA	SA	SA	SB	SC
22,000 pF	223	J	K	M	TA	TB	TC			QB	QB	QC			MA	MA	MA			SA	SA	SA	SB	SB
27,000 pF	273	J	K	M	TA	TB				QB	QB	QC			MA	MA	MA			SA	SA	SA	SC	
33,000 pF	333	J	K	M	TB	TB				QB	QC	QC			MA	MA	MB			SA	SA	SA		
39,000 pF	393	J	K	M	TB	TC				QB	QC	QD			MA	MA	MB			SA	SA	SB		
47,000 pF	473	J	K	M	TB					QB	QC				MA	MB	MC			SA	SA	SB		
56,000 pF	563	J	K	M	TC					QC	QD				MA	MB				SA	SA	SB		
68,000 pF	683	J	K	M						QC	QD				MB	MC				SA	SB	SC		
82,000 pF	823	J	K	M						QC					MB					SA	SB			
0.1 µF	104	J	K	M						QD					MC					SB	SC			
0.12 µF	124	J	K	M											MC					SB				
0.15 µF	154	J	K	M											MC					SC				
Capacitance	Cap Code	Rated Voltage (VDC)			500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000
		Voltage Code			C	B	D	F	G	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G
		Case Size/Series			C2824H					C3040H					C3640H					C4540H				

*Capacitance range Includes E24 decade values only. (i.e., 10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, and 91)

KEMET reserves the right to substitute product with an improved temperature characteristic, tighter capacitance tolerance and/or higher voltage capability within the same form factor (configuration and dimensions).

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Table 2A – Chip Thickness/Tape & Reel Packaging Quantities

Thickness Code	Case Size	Thickness ± Range (mm)	Paper Quantity		Plastic Quantity	
			7" Reel	13" Reel	7" Reel	13" Reel
DG	0805	1.25±0.15	0	0	2,500	10,000
ED	1206	1.00±0.10	0	0	2,500	10,000
EF	1206	1.20±0.15	0	0	2,500	10,000
EG	1206	1.60±0.15	0	0	2,000	8,000
FG	1210	1.25±0.15	0	0	2,500	10,000
FL	1210	1.40±0.15	0	0	2,000	8,000
FM	1210	1.70±0.20	0	0	2,000	8,000
FY	1210	2.00±0.20	0	0	2,000	8,000
FK	1210	2.10±0.20	0	0	2,000	8,000
FS	1210	2.50±0.30	0	0	1,000	4,000
LA	1808	1.40±0.15	0	0	1,000	4,000
LB	1808	1.60±0.15	0	0	1,000	4,000
LC	1808	2.00±0.15	0	0	1,000	4,000
GH	1812	1.40±0.15	0	0	1,000	4,000
GK	1812	1.60±0.20	0	0	1,000	4,000
GM	1812	2.00±0.20	0	0	500	2,000
GO	1812	2.50±0.20	0	0	500	2,000
HE	1825	1.40±0.15	0	0	1,000	4,000
HG	1825	1.60±0.20	0	0	1,000	4,000
HJ	1825	2.00±0.20	0	0	500	2,000
HK	1825	2.50±0.20	0	0	500	2,000
JE	2220	1.40±0.15	0	0	1,000	4,000
JK	2220	1.60±0.20	0	0	1,000	4,000
JL	2220	2.00±0.20	0	0	500	2,000
JN	2220	2.50±0.20	0	0	500	2,000
KE	2225	1.40±0.15	0	0	1,000	4,000
KF	2225	1.60±0.20	0	0	1,000	4,000
KH	2225	2.00±0.20	0	0	500	2,000
KJ	2225	2.50±0.20	0	0	500	2,000
TA	2824	1.40±0.15	0	0	750	2,500
TB	2824	2.00±0.20	0	0	300	2,000
TC	2824	2.50±0.20	0	0	300	2,000
QB	3040	1.40±0.15	0	0	500	1,650
QC	3040	2.00±0.20	0	0	500	1,650
QD	3040	2.50±0.20	0	0	350	1,400
MA	3640	1.40±0.15	0	0	250	1,550
MB	3640	2.00±0.20	0	0	250	1,550
MC	3640	2.50±0.20	0	0	250	1,000
SA	4540	1.40±0.15	0	0	200	1,500
SB	4540	2.00±0.20	0	0	200	1,500
SC	4540	2.50±0.20	0	0	200	1,500
Thickness Code	Case Size	Thickness ± Range (mm)	7" Reel	13" Reel	7" Reel	13" Reel
			Paper Quantity		Plastic Quantity	

Package quantity based on finished chip thickness specifications.

Table 2B – Bulk Packaging Quantities

Packaging Type		Loose Packaging		Secure Packaging		
		Bulk Bag (default)		2" x 2" Waffle Pack/Tray ³		
Packaging C-Spec ¹		N/A ²		7282/7292		
Case Size		Chip Thickness (mm)	Packaging Quantities (pieces/unit packaging)			
EIA (in)	Metric (mm)		Minimum	Maximum	Minimum	Maximum
0402	1005	All	1	50,000	1	368
0603	1608					368
0805	2012					100
1206	3216	≤ 1.25 (nominal)		126		
1206	3216	> 1.25 (nominal)		50		
1210	3225	All		20,000		1
1808	4520		50			
1812	4532		42			
1825	4564		20			
2220	5650		20			
2225	5664		20			

¹ The "Packaging C-Spec" is a 4-digit code which identifies the packaging type. When ordering, the proper code must be included in the 15th through 18th character positions of the ordering code. See "Ordering Information" section of this document for further details. Product ordered without a packaging C-Spec will default to our standard "Bulk Bag" packaging.

² A packaging C-Spec (see note 1 above) is not required for "Bulk Bag" packaging (excluding Anti-Static Bulk Bag). The 15th through 18th character positions of the ordering code should be left blank. All product ordered without a packaging C-Spec will default to our standard "Bulk Bag" packaging.

³ Also commonly referred to as "Chip Carrier" or "Molded Tray". All tray packaging options offer static protection.

Table 3 – Chip Capacitor Land Pattern Design Recommendations per IPC-7351

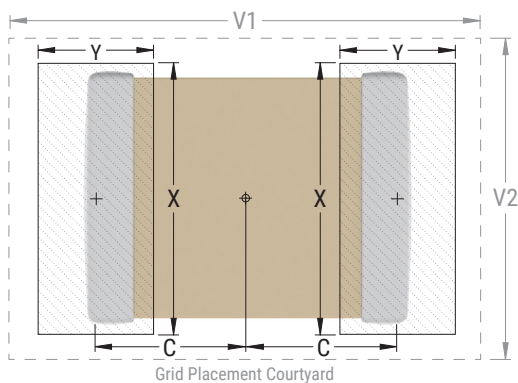
EIA Size Code	Metric Size Code	Density Level A: Maximum (Most) Land Protrusion (mm)					Density Level B: Median (Nominal) Land Protrusion (mm)					Density Level C: Minimum (Least) Land Protrusion (mm)				
		C	Y	X	V1	V2	C	Y	X	V1	V2	C	Y	X	V1	V2
0805	2012	1.00	1.35	1.55	4.40	2.60	0.90	1.15	1.45	3.50	2.00	0.75	0.95	1.35	2.80	1.70
1206	3216	1.60	1.35	1.90	5.60	2.90	1.50	1.15	1.80	4.70	2.30	1.40	0.95	1.70	4.00	2.00
1210	3225	1.60	1.35	2.80	5.65	3.80	1.50	1.15	2.70	4.70	3.20	1.40	0.95	2.60	4.00	2.90
1808	4520	2.30	1.75	2.30	7.40	3.30	2.20	1.55	2.20	6.50	2.70	2.10	1.35	2.10	5.80	2.40
1812	4532	2.15	1.60	3.60	6.90	4.60	2.05	1.40	3.50	6.00	4.00	1.95	1.20	3.40	5.30	3.70
1825	4564	2.15	1.60	6.90	6.90	7.90	2.05	1.40	6.80	6.00	7.30	1.95	1.20	6.70	5.30	7.00
2220	5650	2.75	1.70	5.50	8.20	6.50	2.65	1.50	5.40	7.30	5.90	2.55	1.30	5.30	6.60	5.60
2225	5664	2.70	1.70	6.90	8.10	7.90	2.60	1.50	6.80	7.20	7.30	2.50	1.30	6.70	6.50	7.00
2824	7260	3.45	1.70	6.60	9.60	7.60	3.35	1.50	6.50	8.70	7.00	3.25	1.30	6.40	8.00	6.70
3040	7610	3.70	1.70	10.70	10.10	11.70	3.60	1.50	10.60	9.20	11.10	3.50	1.30	10.50	8.50	10.80
3640	9210	4.45	1.70	10.70	11.60	11.70	4.35	1.50	10.60	10.70	11.10	4.25	1.30	10.50	10.00	10.80
4540	-	5.60	1.70	10.70	13.90	11.70	5.50	1.50	10.60	13.00	11.10	5.40	1.30	10.50	12.30	10.80

Density Level A: For low-density product applications. Recommended for wave solder applications and provides a wider process window for reflow solder processes. KEMET only recommends wave soldering of EIA 0603, 0805 and 1206 case sizes.

Density Level B: For products with a moderate level of component density. Provides a robust solder attachment condition for reflow solder processes.

Density Level C: For high component density product applications. Before adapting the minimum land pattern variations the user should perform qualification testing based on the conditions outlined in IPC Standard 7351 (IPC-7351).

Image below based on Density Level B for an EIA 1210 case size.



Soldering Process

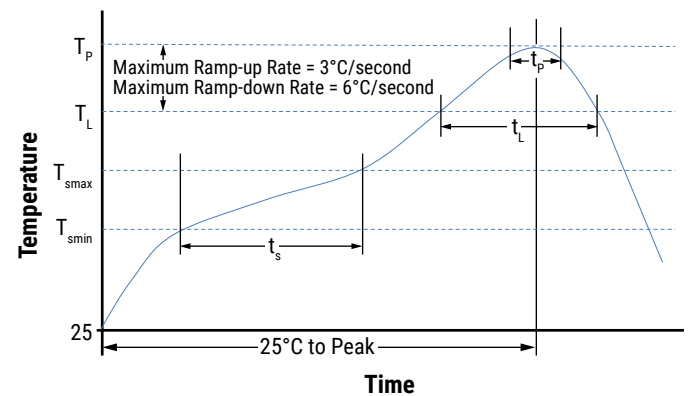
Recommended Soldering Technique:

- Solder wave or solder reflow for EIA case sizes 0603, 0805 and 1206
- All other EIA case sizes are limited to solder reflow only

Recommended Reflow Soldering Profile:

KEMET's families of surface mount multilayer ceramic capacitors (SMD MLCCs) are compatible with wave (single or dual), convection, IR or vapor phase reflow techniques. Preheating of these components is recommended to avoid extreme thermal stress. KEMET's recommended profile conditions for convection and IR reflow reflect the profile conditions of the IPC/J-STD-020 standard for moisture sensitivity testing. These devices can safely withstand a maximum of three reflow passes at these conditions.

Profile Feature	Termination Finish	
	SnPb	100% Matte Sn
Preheat/Soak		
Temperature Minimum (T_{Smin})	100°C	150°C
Temperature Maximum (T_{Smax})	150°C	200°C
Time (t_s) from T_{Smin} to T_{Smax}	60 – 120 seconds	60 – 120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second maximum	3°C/second maximum
Liquidous Temperature (T_L)	183°C	217°C
Time Above Liquidous (t_L)	60 – 150 seconds	60 – 150 seconds
Peak Temperature (T_p)	235°C	260°C
Time Within 5°C of Maximum Peak Temperature (t_p)	20 seconds maximum	30 seconds maximum
Ramp-Down Rate (T_p to T_L)	6°C/second maximum	6°C/second maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum



Note 1: All temperatures refer to the center of the package, measured on the capacitor body surface that is facing up during assembly reflow.

Table 4 – Performance & Reliability: Test Methods and Conditions

Stress	Reference	Test Condition	Limits										
Visual and Mechanical	KEMET Internal	No defects that may affect performance (10X)	Dimensions according KEMET Spec Sheet										
Capacitance (Cap)	KEMET Internal	$C \leq 1,000 \text{ pF}$ Frequency: 1 MHz $\pm 100 \text{ kHz}$ Voltage*: 1.0 V _{rms} $\pm 0.2 \text{ V}$ $C > 1,000 \text{ pF}$ Frequency: 1 kHz $\pm 50 \text{ Hz}$ Voltage: 1.0 V _{rms} $\pm 0.2 \text{ V}$ * See part number specification sheet for voltage	Within Tolerance										
Dissipation Factor (DF)	KEMET Internal	$C \leq 1,000 \text{ pF}$ Frequency: 1 MHz $\pm 100 \text{ kHz}$ Voltage*: 1.0 V _{rms} $\pm 0.2 \text{ V}$ $C > 1,000 \text{ pF}$ Frequency: 1 kHz $\pm 50 \text{ Hz}$ Voltage: 1.0 V _{rms} $\pm 0.2 \text{ V}$ * See part number specification sheet for voltage	Within Specification Dissipation factor (DF) maximum limit at 25°C = 0.1%										
Insulation Resistance (IR)	KEMET Internal	500 VDC applied for 120 ± 5 seconds at 25°C	Within Specification To obtain IR limit, divide M Ω - μF value by the capacitance and compare to G Ω limit. Select the lower of the two limits: 1,000 megohm microfarads or 100 G Ω .										
Temperature Coefficient of Capacitance (TCC)	KEMET Internal	Capacitance change with reference to +25°C and 0 VDC applied. * See part number specification sheet for voltage <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Step</th> <th>Temperature (°C)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>+25°C</td> </tr> <tr> <td>2</td> <td>-55°C</td> </tr> <tr> <td>3</td> <td>+25°C (Reference Temperature)</td> </tr> <tr> <td>4</td> <td>+125°C</td> </tr> </tbody> </table>	Step	Temperature (°C)	1	+25°C	2	-55°C	3	+25°C (Reference Temperature)	4	+125°C	Within Specification: $\pm 30 \text{ ppm} / ^\circ\text{C}$
Step	Temperature (°C)												
1	+25°C												
2	-55°C												
3	+25°C (Reference Temperature)												
4	+125°C												

Table 4 – Performance & Reliability: Test Methods and Conditions cont.

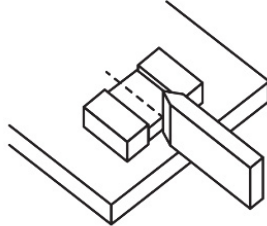
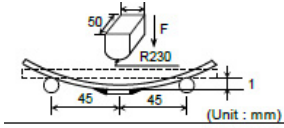
Stress	Reference	Test Condition	Limits						
Dielectric Withstanding Voltage (DWV)	KEMET Internal	150% of rated voltage for voltage rating of < 1,000 V 120% of rated voltage for voltage rating of ≥ 1,000 V (5 ±1 seconds and charge/discharge not exceeding 50 mA)	Cap: Initial Limit DF: Initial Limit IR: Initial Limit Withstand test voltage without insulation breakdown or damage.						
Aging Rate (Maximum % Capacitance Loss/Decade Hour)	KEMET Internal	Maximum % capacitance loss/decade hour	0% Loss/Decade Hour						
Terminal Strength	KEMET Internal	Shear stress test per specific case size, Time: 60 ±1 second. <table border="1" style="display: inline-table; margin-right: 20px;"> <thead> <tr> <th>Case Size</th> <th>Force</th> </tr> </thead> <tbody> <tr> <td>0805</td> <td>9N</td> </tr> <tr> <td>≥ 1206</td> <td>18N</td> </tr> </tbody> </table> 	Case Size	Force	0805	9N	≥ 1206	18N	No evidence of mechanical damage
Case Size	Force								
0805	9N								
≥ 1206	18N								
Board Flex	AEC-Q200-005	Standard Termination System 2.0 mm Flexible Termination System 3.0 mm Test Time: 60± 5 seconds Ramp Time: 1 mm/second 	No evidence of mechanical damage						
Resistance to Soldering Heat	MIL-STD-202 Method 210	Condition B, no per-heat of samples, Single Wave Solder	No evidence of mechanical damage						
Thermal Shock	MIL-STD-202 Method 107	300 cycles (-55°C to +150°C), 20 seconds transfer, 15 minute dwell	Measurement at 24 hours ±4 hours after test conclusion. Cap: Initial Limit DF: Initial Limit IR: Initial Limit						
Temperature Cycling	JESD22 Method JA-104	50 cycles (-55°C to +200°C)	Measurement at 24 hours ±4 hours after test conclusion. Cap: Initial Limit DF: Initial Limit IR: Initial Limit						

Table 4 – Performance & Reliability: Test Methods and Conditions

Stress	Reference	Test Condition	Limits
Biased Humidity	MIL-STD-202 Method 103	Load Humidity: 1,000 hours 85°C/85% RH and 200 VDC maximum Low Volt Humidity: 1,000 hours 85°C/85% RH and 1.5 V.	Measurement at 24 hours ±4 hours after test conclusion. Within Post Environmental Limits Cap: ±0.3% or ±0.25 pF shift IR: 10% of Initial Limit DF Limits Maximum: 0.5%
Moisture Resistance	MIL-STD-202 Method 106	Number of Cycles Required: 10, 24 hours per cycle. Steps 7a and 7b not required	Cap: Initial Limit DF: Initial Limit IR: Initial Limit
Thermal Shock	MIL-STD-202 Method 107	Number of Cycles Required: 5, (-55°C to 125°C) Dwell time 15 minutes.	Cap: Initial Limit DF: Initial Limit IR: Initial Limit
Vibration	MIL-STD-202 Method 204	5 g's for 20 minutes, 12 cycles each of 3 orientations. Test from 10 – 2,000 Hz	Cap: Initial Limit DF: Initial Limit IR: Initial Limit
Mechanical Shock	MIL-STD-202 Method 213	1,500 g's 0.5 millisecond Half-sine, Velocity Change: 15.4 feet/second (Condition F)	Cap: Initial Limit DF: Initial Limit IR: Initial Limit
Resistance to Solvents	MIL-STD-202 Method 215	Add Aqueous wash chemical OKEMCLEAN (A 6% concentrated Oakite cleaner) or equivalent. Do not use banned solvents.	Visual Inspection 10X Readable marking, no decoloration or stains. No physical damage.

Storage and Handling

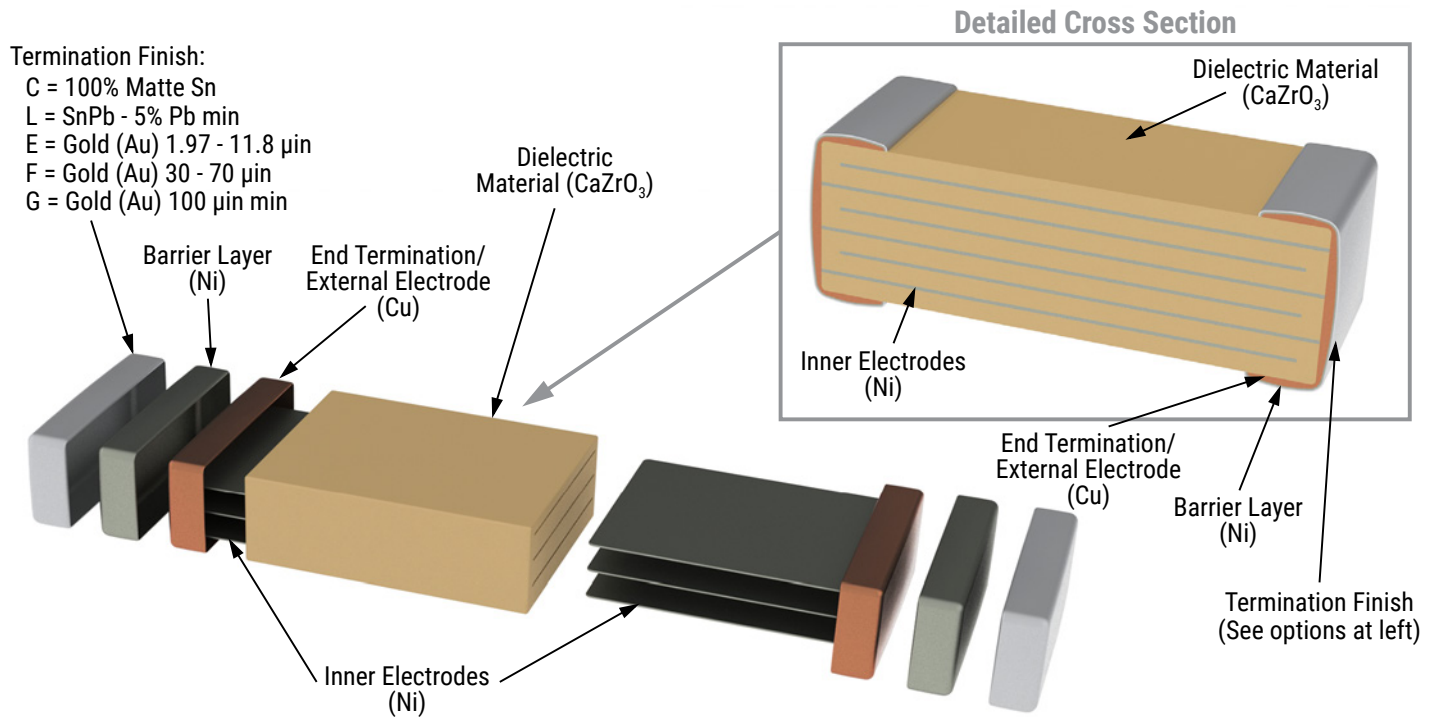
Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature—reels may soften or warp and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C and maximum storage humidity not exceed 70% relative humidity. In addition, temperature fluctuations should be minimized to avoid condensation on the parts and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within the time frame outlined in the table below:

Termination Finish	Termination Finish Ordering Code ¹	Storage Life
100% Matte Tin (Sn)	C	1.5 years upon receipt
SnPb (5% Pb min.)	L	1.5 years upon receipt
Gold (Au) 1.97 – 11.8 µin ²	E	6 months upon receipt ²
Gold (Au) 30 – 70 µin	F	1.5 years upon receipt
Gold (Au) 100 µin min.	G	1.5 years upon receipt

¹ The fourteenth (14th) character position of the KEMET part number is assigned to identify and/or define the termination finish. For more information, see "Ordering Information" section of this document.

² Gold plating option "E" devices should remain in its factory sealed moisture sensitive packaging during storage. If the factory sealed packaging is disturbed please store any remaining packaged components in a dry box container to prevent oxidation of the termination finish.

Construction (Typical)



Capacitor Marking (Optional):

Laser marking option is not available on:

- COG, Ultra Stable X8R and Y5V dielectric devices
- EIA 0402 case size devices
- EIA 0603 case size devices with Flexible Termination option.
- KPS Commercial and Automotive grade stacked devices.

These capacitors are supplied unmarked only.

Tape & Reel Packaging Information

KEMET offers multilayer ceramic chip capacitors packaged in 8, 12, 16 and 24 mm tape on 7" and 13" reels in accordance with EIA Standard 481. This packaging system is compatible with all tape-fed automatic pick and place systems. See Table 2 for details on reeling quantities for commercial chips.

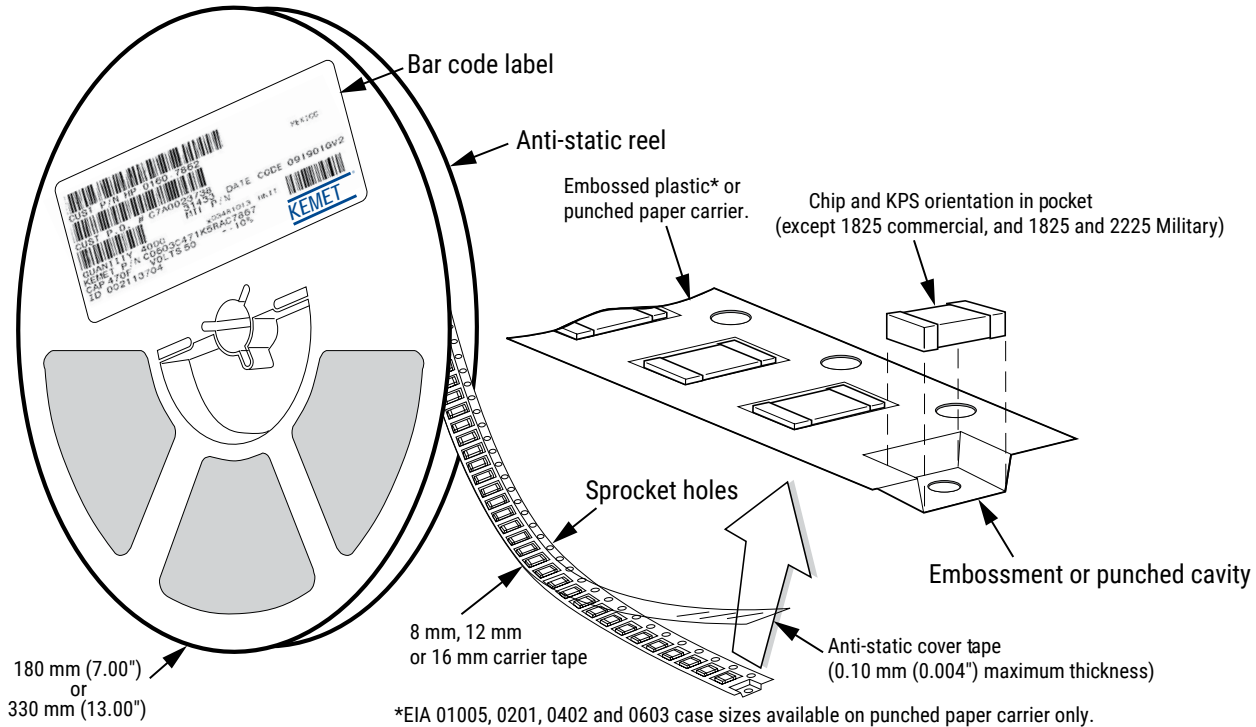


Table 5 – Carrier Tape Configuration, Embossed Plastic & Punched Paper (mm)

EIA Case Size	Tape Size (W)*	Embossed Plastic		Punched Paper	
		7" Reel	13" Reel	7" Reel	13" Reel
		Pitch (P ₁)*		Pitch (P ₁)*	
01005 – 0402	8			2	2
0603	8			4	4
0805	8	4	4	4	4
1206 – 1210	8	4	4	4	4
1805 – 1808	12	4	4		
≥ 1812	12	8	8		
2824	16	12	12		
3040 – 4540	24	16	16		
KPS 1210	12	8	8		
KPS 1812 & 2220	16	12	12		
Array 0508 & 0612	8	4	4		

*Refer to Figures 1 and 2 for W and P₁ carrier tape reference locations.

*Refer to Tables 6 and 7 for tolerance specifications.

Figure 1 – Embossed (Plastic) Carrier Tape Dimensions

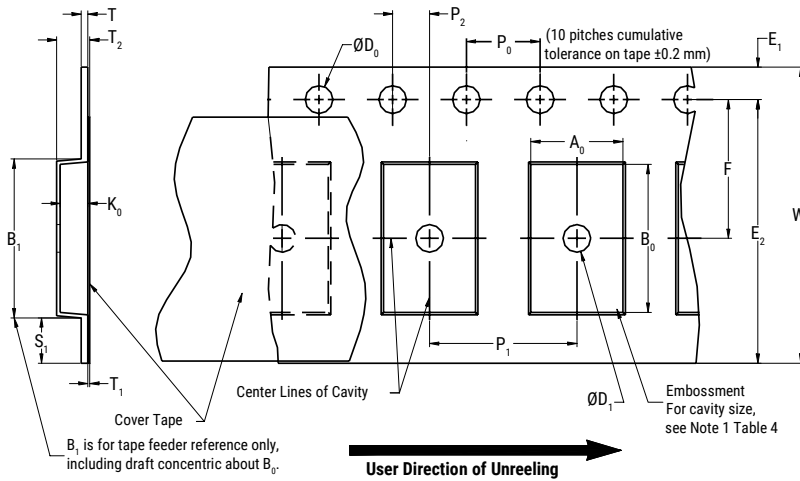


Table 6 – Embossed (Plastic) Carrier Tape Dimensions

Metric will govern

Constant Dimensions – Millimeters (Inches)								
Tape Size	D ₀	E ₁	P ₀	P ₂	R Reference Note 2	S ₁ Minimum Note 3	T Maximum	T1 Maximum
8 mm	1.5+0.10/-0.0 (0.059+0.004/-0.0)	1.75±0.10 (0.069±0.004)	4.0±0.10 (0.157±0.004)	2.0±0.05 (0.079±0.002)	25.0 (0.984)	0.600 (0.024)	0.600 (0.024)	0.100 (0.004)
12 mm					30 (1.181)			
16 mm								
24 mm	1.5+0.10/-0.0 (0.059+0.004/-0.0)	1.75±0.10 (0.069±0.004)	4.0±0.10 (0.157±0.004)	2.0±0.10 (0.078±0.003)	30 (1.181)	5 (0.196)	0.250 (0.009)	0.350 (0.013)
Variable Dimensions – Millimeters (Inches)								
Tape Size	Pitch	E ₂ Minimum	F	P ₁	T ₂ Maximum	W Maximum	A ₀ , B ₀ & K ₀	
8 mm	Single (4 mm)	6.25 (0.246)	3.5±0.05 (0.138±0.002)	4.0±0.10 (0.157±0.004)	2.5 (0.098)	8.3 (0.327)	Note 5	
12 mm	Single (4 mm) & Double (8 mm)	10.25 (0.404)	5.5±0.05 (0.217±0.002)	8.0±0.10 (0.315±0.004)	4.6 (0.181)	12.3 (0.484)		
16 mm	Triple (12 mm)	14.25 (0.561)	7.5±0.05 (0.138±0.002)	12.0±0.10 (0.157±0.004)	4.6 (0.181)	16.3 (0.642)		
24 mm	16 mm	22.25 (0.875)	11.5±0.10 (0.452±0.003)	16.0±0.10 (0.629±0.004)	3 (0.118)	24.3 (0.956)		

- The embossment hole location shall be measured from the sprocket hole controlling the location of the embossment. Dimensions of embossment location and hole location shall be applied independent of each other.
- The tape with or without components shall pass around R without damage (see Figure 6).
- If S₁ < 1.0 mm, there may not be enough area for cover tape to be properly applied (see EIA Standard 481 paragraph 4.3 section b).
- B₁ dimension is a reference dimension for tape feeder clearance only.
- The cavity defined by A₀, B₀ and K₀ shall surround the component with sufficient clearance that:
 - the component does not protrude above the top surface of the carrier tape.
 - the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.
 - rotation of the component is limited to 20° maximum for 8 and 12 mm tapes and 10° maximum for 16 mm tapes (see Figure 3).
 - lateral movement of the component is restricted to 0.5 mm maximum for 8 and 12 mm wide tape and to 1.0 mm maximum for 16 mm tape (see Figure 4).
 - for KPS Series product, A₀ and B₀ are measured on a plane 0.3 mm above the bottom of the pocket.
 - see Addendum in EIA Standard 481 for standards relating to more precise taping requirements.

Figure 2 – Punched (Paper) Carrier Tape Dimensions

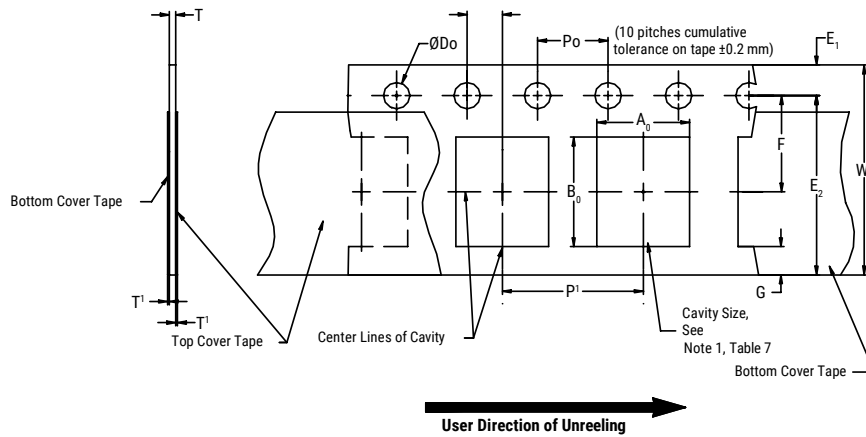


Table 7 – Punched (Paper) Carrier Tape Dimensions

Metric will govern

Constant Dimensions – Millimeters (Inches)							
Tape Size	D_0	E_1	P_0	P_2	T_1 Maximum	G Minimum	R Reference Note 2
8 mm	$1.5+0.10/-0.0$ ($0.059+0.004/-0.0$)	1.75 ± 0.10 (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	2.0 ± 0.05 (0.079 ± 0.002)	0.10 (0.004) Maximum	0.75 (0.030)	2 (0.984)
Variable Dimensions – Millimeters (Inches)							
Tape Size	Pitch	E2 Minimum	F	P_1	T Maximum	W Maximum	$A_0 B_0$
8 mm	Half (2 mm)	6.25 (0.246)	3.5 ± 0.05 (0.138 ± 0.002)	2.0 ± 0.05 (0.079 ± 0.002)	1.1 (0.098)	8.3 (0.327)	Note 1
8 mm	Single (4 mm)			4.0 ± 0.10 (0.157 ± 0.004)			

- The cavity defined by A_0 , B_0 and T shall surround the component with sufficient clearance that:
 - the component does not protrude beyond either surface of the carrier tape.
 - the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.
 - rotation of the component is limited to 20° maximum (see Figure 3).
 - lateral movement of the component is restricted to 0.5 mm maximum (see Figure 4).
 - see Addendum in EIA Standard 481 for standards relating to more precise taping requirements.
- The tape with or without components shall pass around R without damage (see Figure 6).

Packaging Information Performance Notes

- Cover Tape Break Force:** 1.0 Kg minimum.
- Cover Tape Peel Strength:** The total peel strength of the cover tape from the carrier tape shall be:

Tape Width	Peel Strength
8 mm	0.1 to 1.0 newton (10 to 100 gf)
12 and 16 mm	0.1 to 1.3 newton (10 to 130 gf)
24 mm	0.1 to 1.6 newton (10 to 160 gf)

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300 ±10 mm/minute.

- Labeling:** Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. Refer to EIA Standards 556 and 624.

Figure 3 – Maximum Component Rotation

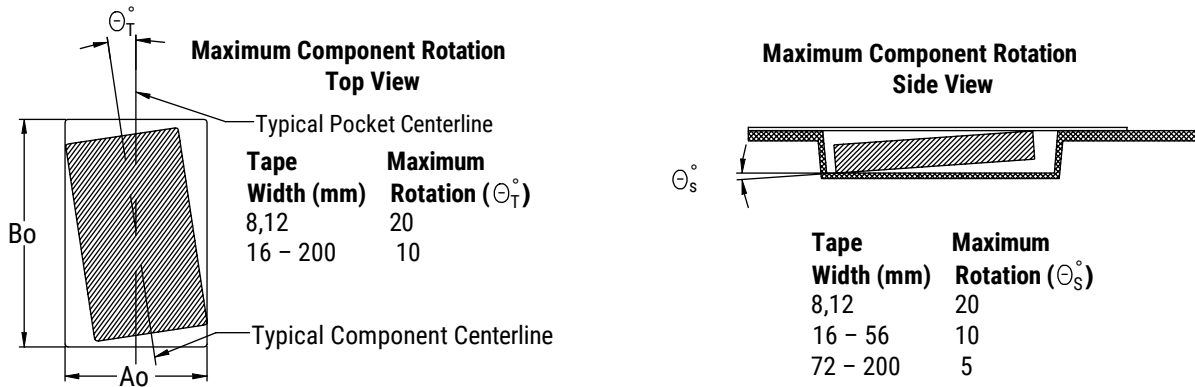


Figure 4 – Maximum Lateral Movement

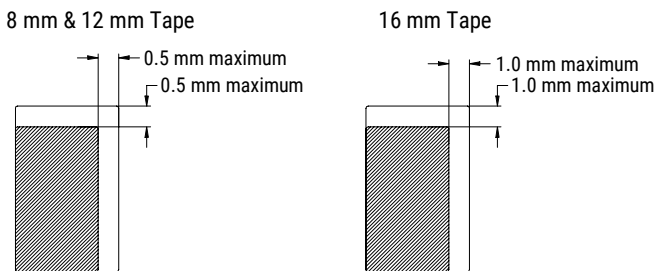


Figure 5 – Bending Radius

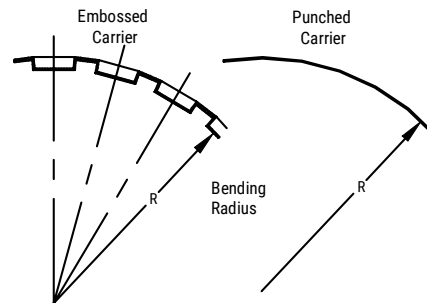


Figure 6 – Reel Dimensions



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Table 8 – Reel Dimensions

Metric will govern

Constant Dimensions – Millimeters (Inches)				
Tape Size	A	B Minimum	C	D Minimum
8 mm	178±0.20 (7.008±0.008) or 330±0.20 (13.000±0.008)	1.5 (0.059)	13.0+0.5/-0.2 (0.521+0.02/-0.008)	20.2 (0.795)
12 mm				
16 mm				
24 mm		1.2 (0.047)	13.0 + -0.2 (0.521 + -0.008)	21 (0.826)
Variable Dimensions – Millimeters (Inches)				
Tape Size	N Minimum	W ₁	W ₂ Maximum	W ₃
8 mm	50 (1.969)	8.4+1.5/-0.0 (0.331+0.059/-0.0)	14.4 (0.567)	Shall accommodate tape width without interference
12 mm		12.4+2.0/-0.0 (0.488+0.078/-0.0)	18.4 (0.724)	
16 mm		16.4+2.0/-0.0 (0.646+0.078/-0.0)	22.4 (0.882)	
24 mm		25+1.0/-0.0 (0.984+0.039/-0.0)	27.4+1.0/-1.0 (1.078+0.039/-0.039)	

Figure 7 – Tape Leader & Trailer Dimensions

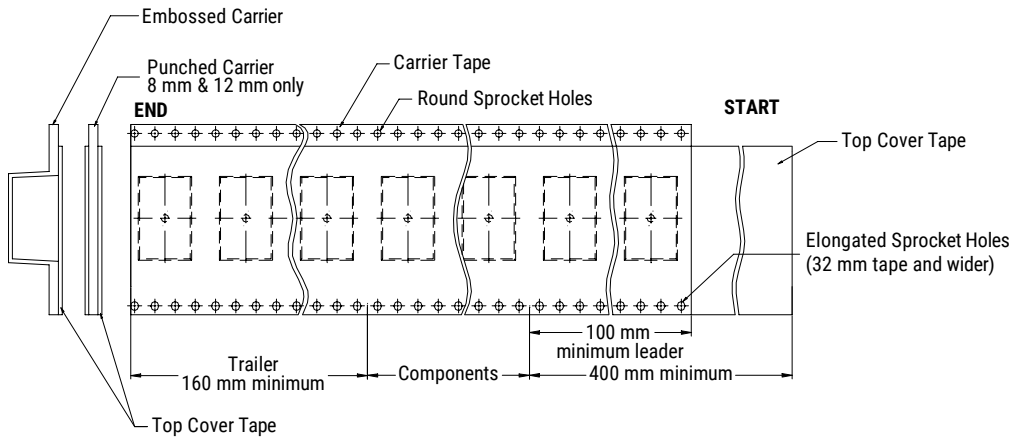
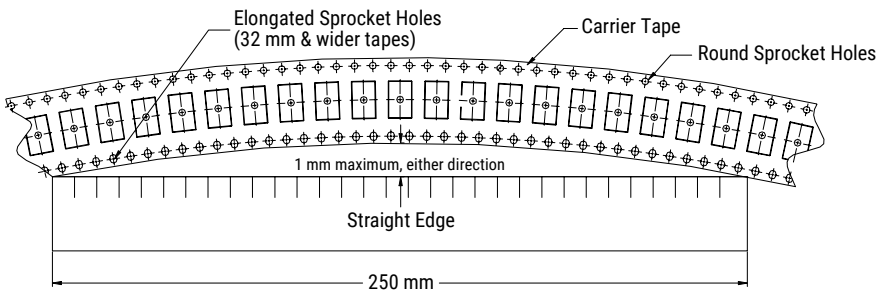


Figure 8 – Maximum Camber



Waffle Tray Packaging Information – 2" x 2" w/ Static Protection

Figure 9 – Waffle Tray Dimensions – Inches (Millimeters)

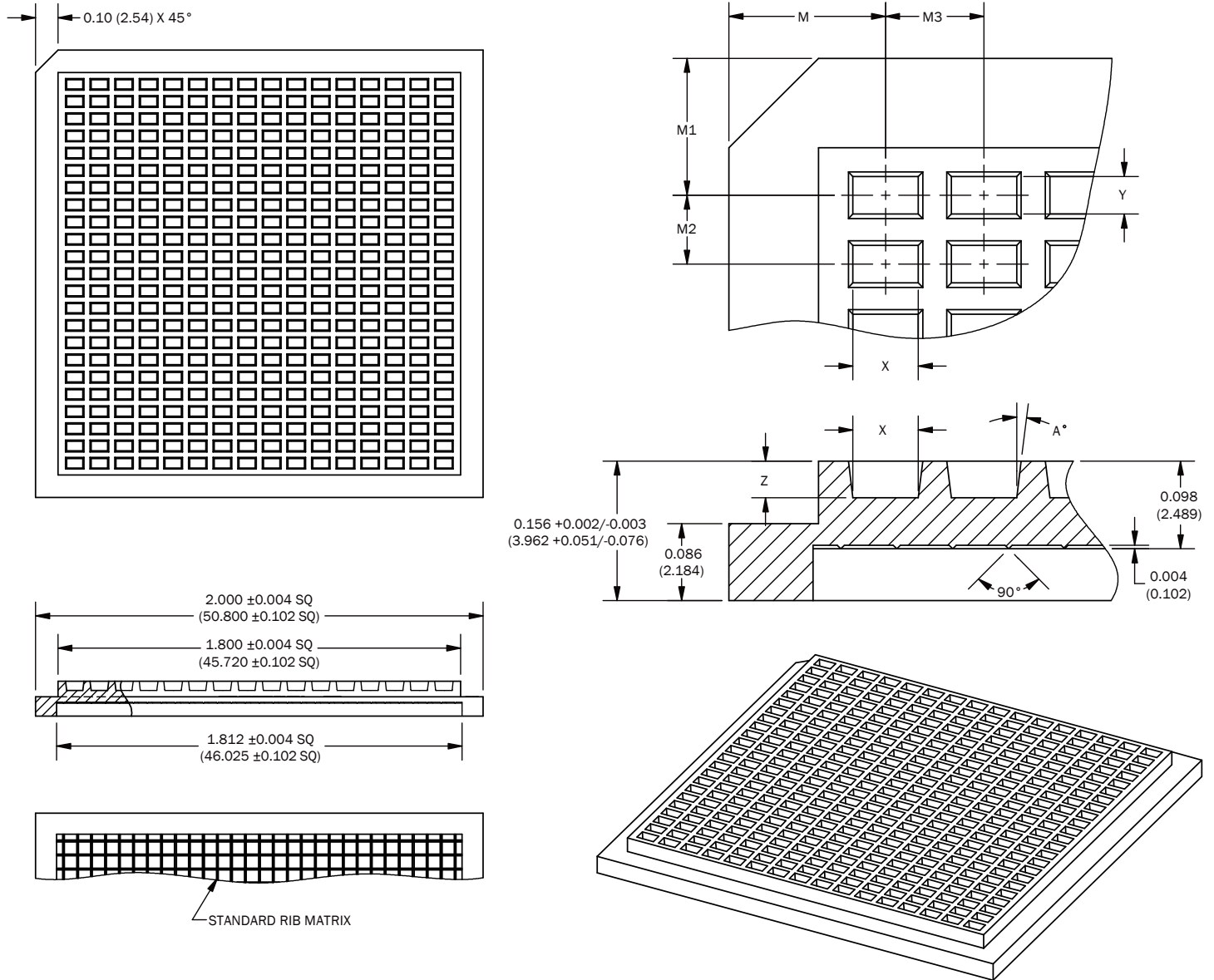


Table 9A – Waffle Tray Dimensions – Inches

Case Size		2" x 2" Waffle Tray Dimensions – Inches									Packaging Quantity (pcs/unit packaging)
		M	M1	M2	M3	X	Y	Z	A°	MATRIX	
EIA (in)	Metric (mm)	±0.003	±0.003	±0.002	±0.002	±0.002	±0.002	±0.003	± 1/2°	(X x Y)	
0402	1005	0.175	0.153	0.077	0.110	0.073	0.042	0.041	7	16 X 23	368
0504	1210	0.235	0.226	0.172	0.170	0.080	0.090	0.055	5	10 X 10	100
0603	1608	0.175	0.153	0.077	0.110	0.073	0.042	0.041	7	16 X 23	368
0805	2012	0.232	0.186	0.181	0.171	0.062	0.092	0.036	10	10 X 10	100
1005	2512	0.230	0.240	0.190	0.140	0.060	0.110	0.075	5	12 X 9	108
1206 ^{1,2}	3216	0.194	0.228	0.193	0.124	0.067	0.130	0.065	5	14 X 9	126
1206 ^{1,3}	3216	0.250	0.250	0.375	0.167	0.100	0.200	0.070	5	10 X 5	50
1210	3225	0.217	0.244	0.215	0.174	0.110	0.145	0.080	5	10 X 8	80
1808	4520	0.271	0.285	0.286	0.243	0.150	0.200	0.075	5	7 X 6	42
1812	4532	0.271	0.285	0.286	0.243	0.150	0.200	0.075	5	7 X 6	42
1825	4564	0.318	0.362	0.424	0.34	0.24	0.32	0.032	5	5 X 4	20
2220	5650	0.318	0.362	0.424	0.34	0.24	0.32	0.032	5	5 X 4	20
2225	5664	0.318	0.362	0.424	0.34	0.24	0.32	0.032	5	5 X 4	20

¹ Packaging of 1206 (3216 metric) case size capacitors is dependent upon the nominal chip thickness of the device. See "Capacitance Range/Selection Waterfall" and "Chip Thickness/Tape & Reel Packaging Quantities" to identify the nominal chip thickness of the capacitor.

² Assigned to 1206 (3216 metric) case size capacitors with nominal thickness of ≤ 1.25mm (0.049 inches).

³ Assigned to 1206 (3216 metric) case size capacitors with nominal thickness of > 1.25mm (0.049 inches).

Table 9B – Waffle Tray Dimensions – Millimeters

Case Size		2" x 2" Waffle Tray Dimensions – Millimeters									Packaging Quantity (pcs/unit packaging)
		M	M1	M2	M3	X	Y	Z	A°	MATRIX	
EIA (in)	Metric (mm)	±0.08	±0.08	±0.05	±0.05	±0.05	±0.05	±0.08	± 1/2°	(X x Y)	
0402	1005	4.45	3.89	1.96	2.79	1.85	1.07	1.04	7	16 X 23	368
0504	1210	5.97	5.74	4.37	4.32	2.03	2.29	1.40	5	10 X 10	100
0603	1608	4.45	3.89	1.96	2.79	1.85	1.07	1.04	7	16 X 23	368
0805	2012	5.89	4.72	4.60	4.34	1.57	2.34	0.91	10	10 X 10	100
1005	2512	5.84	6.10	4.83	3.56	1.52	2.79	1.91	5	12 X 9	108
1206 ^{1,2}	3216	4.93	5.79	4.90	3.15	1.70	3.30	1.65	5	14 X 9	126
1206 ^{1,3}	3216	6.35	6.35	9.53	4.24	2.54	5.08	1.78	5	10 X 5	50
1210	3225	5.51	6.20	5.46	4.42	2.79	3.68	2.03	5	10 X 8	80
1808	4520	6.88	7.24	7.26	6.17	3.81	5.08	1.91	5	7 X 6	42
1812	4532	6.88	7.24	7.26	6.17	3.81	5.08	1.91	5	7 X 6	42
1825	4564	8.08	9.19	10.77	8.64	6.10	8.13	0.81	5	5 X 4	20
2220	5650	8.08	9.19	10.77	8.64	6.10	8.13	0.81	5	5 X 4	20
2225	5664	8.08	9.19	10.77	8.64	6.10	8.13	0.81	5	5 X 4	20

¹ Packaging of 1206 (3216 metric) case size capacitors is dependent upon the nominal chip thickness of the device. See "Capacitance Range/Selection Waterfall" and "Chip Thickness/Tape & Reel Packaging Quantities" to identify the nominal chip thickness of the capacitor.

² Assigned to 1206 (3216 metric) case size capacitors with nominal thickness of ≤ 1.25mm (0.049 inches).

³ Assigned to 1206 (3216 metric) case size capacitors with nominal thickness of > 1.25mm (0.049 inches).

Application Guide

Solder Fluxes and Cleaning

The use of water-soluble fluxes provides advantages of excellent solderability due to high activation. However, these fluxes contain organic acids that can induce arcing under high DC or AC voltages. Notable problem areas are underneath the MLCC where flux can be trapped between the ceramic material and PCB. It is therefore critical that PCBs are properly cleaned to remove all flux residue to maintain reliability.

Coating for High Voltage MLCCs

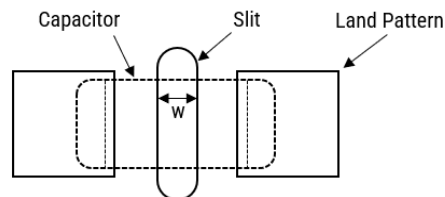
For MLCC ratings $\geq 1500V$, it is recommended to apply a conformal coating to MLCC to prevent surface arcing. To reduce possibility of inducing cracks in the MLCC, select a coating with thermal expansions close to that of the MLCC.

Dielectric	CTE (ppm/°C)
Class II BaTiO ₃	10.7
Class I CaZrO ₃	9.8

Slits in PCB

It is recommended to apply a slit in the PCB under the MLCC to improve washing of flux residue that may get trapped underneath. In some cases, it is not possible to slit entirely through the PCB due to underlying metal planes. It is also acceptable to apply a recessed slit under the MLCC which will also promote cleaning.

- Recommended for case sizes ≥ 1206
- The width (w) of the slit should be 1mm
- Length of the slit should be as short as possible to prevent damaging the MLCC due to mechanical stress of the PCB.
- Slits also reduce the risk of solder balls under MLCC which decreased the creepage distance.



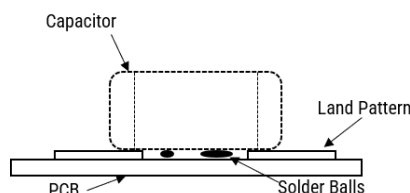
Solder Resist

If a slit cannot be applied as above, it is recommended to not use solder resist directly under the MLCC. The use of solder resist material reduces the distance between MLCC ceramic material and PCB thus making it difficult to clean.

Solder Balls

Improper reflow techniques and/or improper washing can induce solder balls under or adjacent to the MLCC. Solder balls reduce the creepage distance between the MLCC terminations and increase the risk of arcing or damage to the ceramic material. To reduce the risk of solder balls:

- Follow KEMET's solder recommendations as outlined in the datasheet.
- If performing a cleaning procedure, properly clean the PCB per KEMET's cleaning recommendations.
- Add slit to the PCB as shown above.



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